BYOC\_HW6 Simulation 1:

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A.1) Fill up the following table describing what happens in each CK cycle in all instructions. You should specify the specific operations that are required for the execution of the instruction.

We filled in the Rtype and j instructions – as examples. We also gave the list of required registers & signals to be mentioned in the table, in the ori instruction line.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| phase | **IF** | **ID** | **EX** | **MEM** | **WB** |
| Instruction |
| Rtype | IR=IMem[PC]  PC= PC+4 | A=GPR[Rs]  B=GPR[Rt]  Active signals:  RegDst=’1’  RegWrite=’1’  ALUOP=”10”  MemToReg=’0’ | ALUOUT = A op B  Rd is chosen:  Rd\_pMEM=Rd\_pEX | ALUOUT\_pWB=  ALUOUT  (ALUOUT is delayed 1ck) | GPR[Rd\_pWB]  = ALUOUT\_pWB |
| addi |  |  |  |  |  |
| ori | Need to tell what is loaded to IR & PC – the relevant regs. | Again, all regs that are relevant (A, B, sext\_imm, PC in j & branch)  Also – all **active** signals created at the ID phase | All regs that are relevant (ALUOUT, B\_reg\_pMEM, Rd\_pMEM, sext\_imm) | All regs that are relevant (ALUOUT\_reg\_bWB, Rd\_pWB, MDR)  MDR= DMem[adrs ] or  DMem[adrs]=B\_reg\_pMEM | GPR[Rd\_pWB]  = ALUOUT\_pWB |
| lui |  |  |  |  |  |
| beq |  |  |  |  |  |
| bne |  |  |  |  |  |
| lw |  |  |  |  |  |
| sw |  |  |  |  |  |
| j | IR=IMem[PC]  PC=PC+4 | PC= jump adrs | nothing | nothing | nothing |
| jal |  |  |  |  |  |
| jr |  |  |  |  |  |

Answer the following questions.

A.2) Describe the changes done in order to support the ORI instruction.

A.3) Describe the changes done in order to support the LUI instruction.

A.4) Describe the changes done in order to support the JR instruction.

A.5) Describe the changes done in order to support the JAL instruction.

In your answers, besides stating the reasoning in detail, show the relevant VHDL code sections to better explain your answers.